Claim Amendments

1. (Currently amended)   A method for evaluating measured data utilizing analog-to-digital conversion so as to obtain digitalized measured data from analog measured data, disseminating said digitalized measured data to a digital signal processor for processing said digitalized measured data by computation, and outputting respective measured values from the processor, the improvement comprising:

utilizing a shift register between commonly ~~connected~~ connecting outputs of a plurality of analog-to-digital converters ~~and~~ to said digital signal processor by interfacing said outputs with a shift register interposed between the converters and said digital signal processor,

intermediately storing in said shift register digitalized measured data produced by said converters from analog measured data until all digitalized measured data to be processed is acquired in the shift register,

reading out in a block transfer from the shift register all digitalized measured data to be processed, and

simultaneously processing in said digital signal processor digitalized measured data read out from the shift register to obtain respective measured values.

2. (Currently amended)   A device for obtaining measured values by evaluating measured data, including a plurality of analog-to-digital converters ~~having a common output connection and~~ configured to digitalize analog measured data applied to the converters, ~~and~~ a digital signal processor configured to simultaneously process digitalized measured data by computing to obtain respective measured values, and a shift

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register arranged between said ~~common output connection of the~~ plurality of analog-to-digital converters and said digital signal processor, the digitalized measured data from the outputs of the analog-to-digital converters being commonly connected to the shift register by interfacing, said register being configured to intermediately store said measured digitalized data ~~upon digitalization~~ until all digitalized measured data to be processed simultaneously is acquired by the register for block transfer to the digital signal processor.

3. (Original) A device as set forth in claim 2, wherein said shift register is designed as a FIFO memory.

4. (Original) A method as set forth in claim 1, wherein said shift register is designed as a FIFO memory.